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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,429	12/29/2000	Robert M. Reinschmidt	CY-0018	7651

7590 09/21/2005

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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,429	REINSCHMIDT ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5 and 21* is/are allowed.

6)☒ Claim(s) *8-20* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Application filed on 12/29/2000. Claims 1-21 are pending.

Drawings

2. Figures 7, 8, 9, 10, 11, 12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see Applicant's specification, pages 2-4). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: bit circuit 800 not shown in Fig. 8 (page 2, lines 14-15). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. **Claims 6-14,16-19** are objected to because of the following informalities:

As per **claim 6**, "the upward contacts" (line 2) should be --upward contacts-- for greater clarification and for proper antecedent basis since "upward contact" (singular form) was previously cited.

As per **claim 7**, "the lower contacts" (line 2) should be --lower contacts-- for greater clarification and for proper antecedent basis since "lower contact" (singular form) was previously cited.

As per **claim 8**, "that each provide" (line 2) should be --in which each ID bit circuit provides--for greater clarification and for proper grammar; "can" (line 4) should be deleted to clearly identify what is being claimed.

As per **claim 13**, "the potential" (line 2) should be --potential-- for proper antecedent basis; "the sense" (line 3) should be --sense-- for proper antecedent basis.

As per **claim 14**, "can" (line 2) should be deleted to clearly identify what is being claimed.

As per **claims 9-14**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 16**, "the upward contacts" (line 4) should be -- wherein upward contacts-- for proper antecedent basis and for greater clarification; ", the downward

contacts" (line 5) should be --and downward contacts-- for proper antecedent basis and for greater clarification.

As per **claim 17**, "the orientation" (line 3) should be --orientation-- for proper antecedent basis.

As per **claim 18**, the claim is objected to for incorporating the above error into the claim by claim dependency.

As per **claim 19**, "the same" (line 4) should be --a same-- for proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 8-20** are rejected under 35 U.S.C. 102(a) or (b) as being anticipated by Applicant's admission of prior art (see Applicant's specification, page 1, line 8 to page 4, line 18).

As per **claims 8,14**, all of the elements of the claims are described in Applicant's admission of the prior art as discussed in Applicant's specification, page 2, lines 3-13

which are illustrated in Fig. 7, wherein n mask identification bit circuits corresponds to the ID bit circuits 702-0...702-n, wherein n is the integer including being greater than 1 as illustrated in Fig. 7, in which each circuit provides one bit of a mask identification code corresponding to each output SA0...SAn, wherein the output bits SA0...SAn, together provides the more than n different mask identification codes since each bit can have a value of "0" or "1", the combination of n-bits (SA0...SAn) would inherently provide for 2^n different or unique values for mask identification codes.

As per **claim 9**, all of the elements are discussed in the rejection of claim 8, from which the claim depends, wherein Applicant's admission of prior art further describes the elements of the claims in Applicant's specification, page 3, line 14 to page 4, line 1, and illustrated in Fig. 8, each mask ID bit SAn include a sense node 804, being coupled to one of at least two different potentials (VGND or VPWR) by at least two signal paths as shown by the lines (i.e., links 802-0, 802-1, 802-2, 802-3, 802-4) connecting the inputs VGND and VPWR to the output SAn in Fig. 8.

As per **claim 10**, all of the elements are discussed in the rejection of claim 8, from which the claim depends, wherein Applicant's admission of prior art further describes the elements of the claims as shown in Fig. 8, wherein each mask ID bit SAn include a sense node 804, being coupled to one of at least two different potentials (i.e., a first and a second potential--VGND and VPWR) by at least two signal paths as shown by the lines (i.e., links 802-0, 802-1, 802-2, 802-3, 802-4) connecting the inputs VGND and VPWR to the output SAn in Fig. 8, wherein the output bits SA0...SAn, together provides the more than n different mask identification codes (as discussed in the

rejection of claim 8 above), thus identifying a first mask, a second mask, a third mask, up to 2^n masks using the combination of these two potentials.

As per **claim 11**, all of the elements are discussed in the rejection of claim 8, from which the claim depends, wherein Applicant's admission of prior art further describes the elements of the claims as shown in Fig. 8, wherein since there are several switches (i.e., double throw switches--see Applicant's specification, page 2, line 22 to page 3, line 1) between the inputs lines (VGDN and VPWR) and the output line (SAn) to identify the different mask (see the rejection of claim 8), these separate signal paths in combination with the switches would inherently include separate paths that are cross coupled with one another (i.e., one or more double throw switches connecting from VGND line to VPWR line).

As per **claim 12**, all of the elements are discussed in the rejection of claim 8, from which the claim depends, wherein Applicant's admission of prior art also describes the plurality of links, each link being formed on a different integrated circuit layer (see Applicant's specification, page 2, lines 14-21).

As per **claim 13**, all of the elements are discussed in the rejection of claim 12, from which the claim depends, wherein Applicant's admission of prior art further describes each link switching the potential supplied to the sense node (i.e., acting as double throw switches--Applicant's specification page 2, line 22 to page 3, line 1), wherein as illustrated in Fig. 8, each link comprises two conductive line segments, one conductive segment connecting a solid dot to a open dot of another link, and another conductive segment connecting the solid dot to one of two open dots to provide for the

desired first or second configuration (i.e., connected or set to the potential line VGND or VPWR).

As per **claim 15**, all of the elements of the claims are described in Applicant's admission of the prior art as discussed in Applicant's specification, page 2, lines 3 to page 3, line 17, which are illustrated in Figs. 7, 8, and 9, wherein mask identification bit circuits corresponds to the ID bit circuits 702-0...702-n wherein n is the integer including being greater than 1 as illustrated in Fig. 7; in which each circuit is formed as illustrated in Figs. 8 and 9, having interconnected links on a plurality of layers (i.e., links 802-0, 802-1, 802-3, 802-4, see page 2, lines 14-21 and page 3, lines 2-17) that provide a signal path to a sense node (i.e., 804); wherein each link being switchable between at least two configurations are illustrated in Fig. 8, wherein each link switching the potential supplied to the sense node (i.e., acting as double throw switches--Applicant's specification page 2, line 22 to page 3, line 1), through a series of conductive segments (i.e., Fig. 8 shows each link comprises two conductive line segments, one conductive segment connecting a solid dot to a open dot of another link, and another conductive segment connecting the solid dot to one of two open dots) to provide for the desired first or second configuration (i.e., connected or set to the potential line VGND or VPWR); wherein each ID bit circuit together forms the mask bit identification (ID) circuits which provide for up to 2^n unique or different mask identification codes (see rejection of claim 14 above), representing the multiple mask changes.

As per **claim 16**, all of the elements of claim 15, from which the claim depends, are discussed in the rejection of claim 15 above, wherein the interconnect links having

upward and downward contacts are also discussed in Applicant's admission of prior art as further described in Applicant's specification, page 3, lines 7-17, wherein since the contacts are arranged as shown in Fig. 8, a crossing connection from signal line VGND to VPWR at the switching points would necessary create diagonal lines connections, and these diagonal lines are essentially diagonal to one another.

As per **claim 17-19**, all of the elements of claim 15, from which the claim depends, are discussed in the rejection of claim 15 above, wherein the switching of more than one link and switching of the configuration are also discussed in Applicant's admission of prior art as further described in Applicant's specification, page 3, line 2 to page 4, line 18, wherein such changing of the conductive orientations are basically changing connections in the double throw switches such that conductive lines (segments) are oriented in different positions (i.e., vertical, horizontal, diagonal), wherein since vertical and horizontal connections are allowed (page 3, lines 2-6; Fig. 8), two conductive lines can be placed essentially perpendicular to a previous orientation.

As per **claim 20**, all of the elements of claim 15, from which the claim depends, are discussed in the rejection of claim 15 above, wherein the further limitations of the claims are also discussed in Applicant's admission of prior art as described in Applicant's specification, page 2, lines 16-21.

Allowable Subject Matter

7. **Claims 1-5,21** are allowed.

8. **Claims 6-7** would be allowable if rewritten to overcome the minor informalities set forth in this Office action.

9. The following is a statement of reasons for the indication of allowable subject matter:

As per **claims 1-7**, the independent claim 1, from which the claims depend, recites the mask identification circuit comprising the inventive features of having the inputs being cross coupled to the outputs for each link, in a second configuration, in addition to the inputs being directly coupled to the outputs for each link, in a first configuration, as part of the plurality of links arranged in series, as claimed, which the prior arts made of record failed to teach or suggest. In particular, although Applicant's admission of the prior art teach direct coupling of the inputs to the outputs in each link (see Applicant's specification, Fig. 8), cross coupling between inputs and outputs for each link is not possible. Other prior arts made of record teach various methods/systems for implementing identification circuits (see especially **Genetti et al.**, US Patent Application Publication No. 2003/0177468, especially paragraphs [0004], [0024], [0040]; **Debenham et al.**, U.S. Patent No. 6,365,421, especially col. 8, line 60 to col. 10, line 59; **Zheng et al.**, U.S. Patent No. 5,895,962, especially col. 4, line 44 to col. 6, lie 37). However, none of the prior arts made of record, alone or in combination, teaches the inventive features as claimed. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

As per **claim 21**, the claim recites a mask revision identification (IC) code circuit, comprising means functional language of the claim, which corresponds to Applicant's specification, page 7, line 13 to page 13, line 18, for cross coupling at least two signal lines according to changes in at least two circuit masks to generate a mask ID code bit,

as claimed, which the prior arts made of record failed to teach or suggest as claimed. In particular, although Applicant's admission of the prior art teach connection can be make from a first signal line (i.e., top conductive line) to a second signal line (i.e., bottom conductive line) using any one of the double throw switches (see Applicant's specification, Fig. 8), the bottom signal line cannot take the value of the top signal line to generate a mask ID code bit, as claimed; thus no cross coupling of the at least two signal lines are possible. Other prior arts made of record as discussed in the reasons for allowable subject matter of claims 1-7 above, alone or in combinations with the prior arts made of record, similarly failed to teach or suggest the inventive features as claimed. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is herein requested to consider them carefully in response to this Office Action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 8:30AM-7PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik
U.S. Patent Examiner
September 15, 2005